

Notice of References Cited	Application/Control No. 10/643,193		Applicant(s)/Patent Under Reexamination BHAVNAGARWALA ET AL.	
	Examiner Jeffrey R. West		Art Unit 2857	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,275,094	08-2001	Cranford et al.	327/534
*	B	US-6,731,916	05-2004	Haruyama, Shinichi	455/194.2
*	C	US-5,999,043	12-1999	Zhang et al.	327/558
*	D	US-6,819,183	11-2004	Zhou et al.	330/289
*	E	US-4,851,768	07-1989	Yoshizawa et al.	324/751
*	F	US-6,181,621	01-2001	Lovett, Simon J.	365/205
*	G	US-6,798,278	09-2004	Ueda, Yoshinori	327/541
*	H	US-2004/0193390	09-2004	Drennan et al.	703/002
*	I	US-6,628,146	09-2003	Tam, Simon	327/63
*	J	US-6,161,213	12-2000	Lofstrom, Keith	716/4
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
*	U	Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime", Proceedings of the IEEE 1997 Int Conference on Microelectronic Test Structures, Vol. 10, March 1997.			
*	V	Bastos et al., "Mismatch characterization of small size MOS transistors", Proceedings of the IEEE 1995 Int. Conference on Microelectronic Test Structures, Vol. 8, March 1995.			
*	W	Shen et al., "Down Literal Circuit with Neuron-MOS Transistors and Its Applications", Proceedings. 1999 29th IEEE International Symposium on Multiple-Valued Logic, 20-22 May 1999 Page(s):180 - 185.			
*	X	Lakshmikumar et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design", IEEE Journal of Solid-State Circuits, Vol. 21, Issue: 6, Dec 1986.			

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 10/643,193	Applicant(s)/Patent Under Reexamination BHAVNAGARWALA ET AL.	
	Examiner Jeffrey R. West	Art Unit 2857	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Pavasovic et al., "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems", Journal of VLSI Signal Processing, 8, 75-85, 1994.
*	V	Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability", IEEE Journal of Solid-State Circuits, Vol. 36, No. 4, April 2001.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.